

REMARKS**Claim Rejections Under 35 U.S.C. § 112**

Claim 4 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 4 has been canceled.

Claim Rejections Under 35 U.S.C. § 102 and 35 U.S.C. § 103

Claims 1, 6, 8-10, and 15 were rejected under 35 U.S.C. § 102(b) as being anticipated by *Haukka et al.* (U.S. Patent No. 6,660,660), or in the alternative under 35 U.S.C. § 103(a) as being obvious over a prior art device - for example a device disclosed by *Hoefler et al.* (U.S. Patent No. 6,713,812) in view of *Haukka et al.* Applicant respectfully traverses this rejection.

Haukka et al. disclose an integrated circuit structure comprising aluminum oxide or lanthanide layers formed by atomic layer deposition (ALD). A high-k dielectric material is formed between these layers. *Hoefler et al.* disclose a memory device having a SONOS structure. However, neither *Haukka et al.* nor *Hoefler et al.* teach or suggest Applicant's structures as claimed in the amended claims.

Haukka et al. teach that the dielectric must have an oxide material on either side of a high-k layer. It is well known in the art that the oxide layer is one of a silicon dioxide, aluminum oxide, or lanthanide oxide and neither *Haukka et al.* nor *Hoefler et al.* teach or suggest otherwise. Applicant's structures, as claimed in the amended claims, have a nanolaminate structure that does not use these oxides. Applicant's amended claims 6 and 15 use HfO₂ on either side of a high-k layer. Applicant's amended claim 1 uses a Al₂O₃, HfO₂, or ZrO₂ layer under the nitride layer. Neither *Haukka et al.* nor *Hoefler et al.* teach or suggest such a composition for a nanolaminate layer.

CONCLUSION

For the above-cited reasons, Applicant respectfully requests that the Examiner allow the claims of the present application. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

Date: _____

3/15/05

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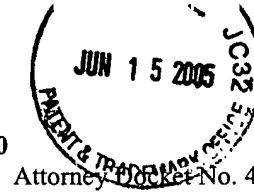
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REPLY UNDER 37 CFR 1.116 –

EXPEDITED PROCEDURE – TECHNOLOGY CENTER 2800

Serial No. 10/775,908

Title: NROM FLASH MEMORY WITH A HIGH-PERMITTIVITY GATE DIELECTRIC



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Attorney Docket No. 400.272US01

AMENDMENTS TO THE DRAWINGS

The drawings were objected to as failing to comply with 37 CFR 1.83(a). The Examiner stated that the p+ silicon material was not shown. However, Figure 1, reference 103 shows the p-type silicon substrate and this is further described in paragraph 20 of the specification. Even though the label “p+” is not present in the drawings, the silicon substrate 103 is clearly shown in the drawings and the specification describes the different types of silicon conductivity encompassed by the present invention. Additionally, it would be well known by those skilled in the art that if the active areas 101 and 102 are n-type silicon as labeled in Figure 1, the substrate is going to be p-type silicon (and vice versa).